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Subthreshold Dual Mode Logic

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Abstract

In this brief, we introduce a novel low-power dual mode logic (DML) family, designed to operate in the subthreshold region. The proposed logic family can be switched between static and dynamic modes of operation according to system requirements. In static mode, the DML gates feature very low-power dissipation with moderate performance, while in dynamic mode they achieve higher performance, albeit with increased power dissipation. This is achieved with a simple and intuitive design concept. SPICE and Monte Carlo simulations compare performance, power dissipation, and robustness of the proposed DML gates to their CMOS and domino counterparts in the 80-nm process. Measurements of an 80-nm test chip are presented in order to prove the proposed concept.

Keywords*: Dual mode logic (DML), low power, subthreshold*

1. Introduction

With advancements in technology and the expansion of mobile applications, power consumption has become a primary focus of attention in VLSI digital design [1]–[2]. Recently, digital subthreshold circuit design has become a very promising method for ultralow power applications [1], [3]. Circuits, operating in the subthreshold region, utilize a supply voltage (*V*DD*)* that is less than the threshold voltages of the transistors, which allows significant reduction of both dynamic and static power. However, an aggressive scaling of supply voltage also results in performance degradation and a much higher sensitivity to process variations and temperature fluctuations [4], [5]. The most common logic design family used for subthreshold today is CMOS. Ultralow voltage operation, which offers low-tomoderate performance with ultralow power dissipation, was examined for the first time in 1972 [6] and was originally used for lowthroughput applications such as wrist watches, biomedical devices, and sensors [7]. Dynamic logic, such as domino logic, has been used since the 1970's for high-performance applications [8]. In the past, there have been several attempts to use dynamic logic in subthreshold to improve the speed [9]. However, these attempts did not gain momentum because of high sensitivity to process variations in nanoscale technologies. In this brief, we propose a novel logic family, dual mode logic (DML), designed to operate in the subthreshold region. The proposed logic can be operated in two modes: static CMOS-like mode and dynamic np-CMOS-like mode (which will be referred to as a dynamic mode). In the static mode, the DML gates feature very low power dissipation with moderate performance, while in the dynamic mode, they achieve much higher performance, albeit with increased power dissipation. This unique feature of the DML provides the option to control system performance on-the-fly and thus support applications in which a flexible workload is required.

DML shows high immunity to process variations, making it possible to operate DML gates from a supply voltage as low as 300 mV. Simulations, performed on chains of basic NAND/NOR gates, indicate that while operating in the dynamic mode, subthreshold DML achieves an improvement in speed of up to 10× compared to a standard CMOS, while dissipating 1.5× more power. In the static mode, a 5× reduction of power dissipation is achieved, compared to a basic domino, at the expense of a magnitude decrement in performance. Monte Carlo simulations of DML present a significant improvement in robustness, as compared to domino logic. The rest of this brief is constructed as follows. Section II presents an overview of the basic DML logic gate and method of operation. A comparison of DML speed,

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energy dissipation, and robustness with CMOS and dynamic logic are shown in Section III through simulations and test chip measurements. Section IV concludes this brief.

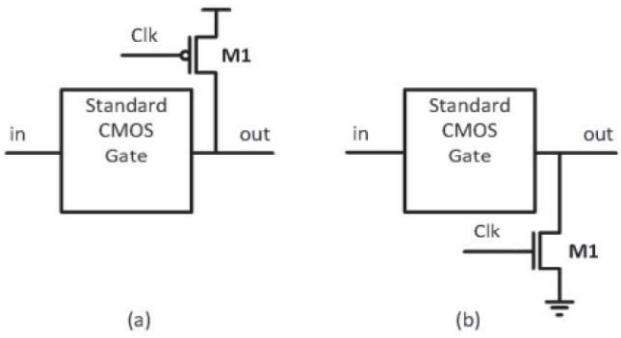


Figure 1. Proposed basic DML gate. (a) Type A topology. (b) Type B topology.

2. DML Structure and Principle of Operation

The basic DML gate architecture is composed of a standard CMOS gate and an additional ransistor M1, whose gate is connected to a global clock signal, as shown in Figure 1. At first glance, this architecture is very similar to the noise tolerant precharge (NTP) structure, introduced by Yamada *et al.* [10]. However, in contrast to the NTP, which was developed as a high-speed, high-noise-tolerance dynamic logic, the DML aims to allow operation in two functional modes: static mode and dynamic mode. To operate the gate in the dynamic mode, the Clk is assigned an asymmetric clock, allowing two distinct phases: precharge and evaluation. During the precharge phase, the output is charged to high/low, depending on the topology of the DML gate. In the consequent evaluation phase, the output is evaluated according to the values at the gate inputs. The proposed DML topologies, marked *Type A* and *Type B*, are illustrated in Figure 1. Type A has an added p-MOS transistor that precharges the output to a logical "1" during the precharge phase.

Type B has an added n-MOS that precharges the output to a logical "0." Dynamic logic gates are often implemented using a footer, which requires an additional transistor. The footer is used to decrease precharge time by eliminating the ripple effect of the data advancing through the cascaded nodes and allowing faster precharge.

Switching the DML gate to operate in CMOS-like (i.e., static mode) operation is fairly intuitive: the global Clk should be fixed high for Type A topology and constantly low for Type B topology. As a result, the gate attains a similar topology to CMOS, except for the extra parasitic capacitance, which is usually negligible. Creating a DML node based on a CMOS gate is also very simple: "gluing" an additional transistor for the precharge phase, and, in the case of a footed gate, adding an additional n-MOS transistor as a footer in Type A gates and a p-MOS transistor as a header in Type B gates.

In addition to the unique capability to switch between different modes of operation, DML nodes which are operating in dynamic mode have a number of salient advantages over conventional dynamic nodes, which stem from the DML topology. The DML inherently features an active keeper constructed of the CMOS complementary logic. The active keeper is derived from the structure of the node, in which the CMOS part is still fully functional, and assists in maintaining the output level. This is the key attribute to the immunity to process variations, temperature fluctuations, and solving some of the domino's well known drawbacks such as charge sharing, crosstalk noise, and susceptibility to glitches, which intensify with process and voltage scaling. The design methodology that should be used when designing a DML gate is to place the precharge transistor in parallel to the stacked transistors. Thus, the evaluation is performed with the parallel transistors and, therefore, it is faster. The stacked transistors will be sized to minimal widths to reduce intrinsic capacitances, increasing dynamic operation performance over reduced static operation performance. This sizing strategy also results in reduced energy dissipation, as compared to conventional static CMOS gates. The precharge transistor is also minimum sized to decrease leakage currents during static operation and

evaluation. Note, all gates can be designed either as Type A or Type B, ignoring the optimization guidelines mentioned above. The optimal design methodology when designing with DML gates is to cascade connect Type A and Type B gates, exactly like in np-CMOS gates. Even though this design methodology will allow maximum performance, minimize area, and maximize power efficiency, it is possible to connect gates of the same type by using an inverter buffering between them, in a similar way it is done in domino logic. Connecting gates of the same type without inverters is also possible when a footer/header is used at each stage, however, this structure will cause glitching after precharge ends and until the evaluation data ripples through the chain. These are standard problems when designing with dynamic gates [11]. However in contrast to the standard dynamic logic, DML's inherent keeper helps recover the logical value.

3. Comparative Performance Analysis through Simulations and Measurements

We compared DML gates to their CMOS and domino counterparts by means of speed, power, and robustness. All the test gates were examined and characterized in a standard low-power 80- nm process, using the Cadence Virtuoso-based Spectre simulator. Power supplies between 150 mV and 600 mV were tested for energy estimation. Monte Carlo statistical simulations were performed at 300 mV to compare the sensitivity of the simulated gates to process variations and mismatch. The DML gates, tested in the rest of this brief, are unfooted, except for Section III-C, where the comparison of the footed DML gates to their footed dynamic counterparts is presented. In cases of DML gates without footers, the simulation results include the overhead of generating the ripple precharge signals. In order to provide a fair comparison, the same metric was used to design all gates (CMOS, domino, and DML). All gates were designed to conduct the same Ion current during evaluation. This current is equal to the Ion current flowing through a single transistor of a CMOS inverter.

3.1. Speed

We setup a framework for evaluating frequency consisting of fanout three NAND and NOR gates. We compared standard CMOS gates, unfooted DML gates, and domino gates both with and without a.

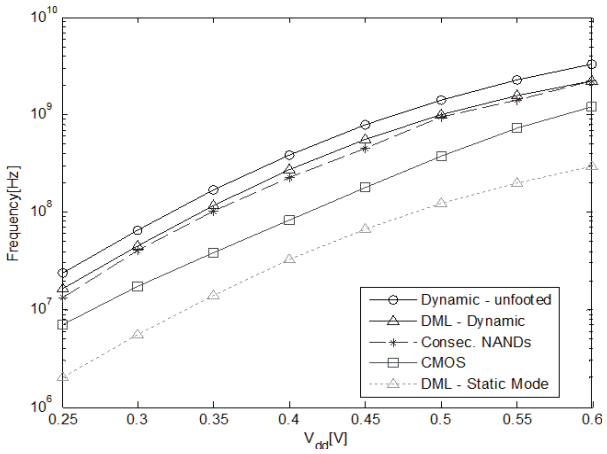


Figure 2. Simulated speed for CMOS, domino, and DML (static and dynamic)

FO-3 NAND-NOR chain and for DML FO-3 NAND-NAND chain keeper. The role of the keeper in receiving acceptable robustness will be discussed in Section III- C. A test chain was composed of 20 consecutive NAND and NOR gates, in which the NOR gate was implemented in A topology, and NAND was implemented in B topology, laying a similar structure to an np-CMOS design. While this np-CMOS-like chain demonstrated better results, we also show the performance of consecutive DML gates of the same type. We tested the minimal functional

period *T* of the entire chain, in which *T* is defined in (1), and the operation frequency of the entire chain is *f=1/T*

$$T = \frac{t_{HL} + t_{LH}}{2} \quad (1)$$

After the precharge phase, the output of a dynamic NOR gate is high, and when no switching occurs, it literally gives *t*plh = 0. When switching does occur, the output capacitance *CL* is discharged through the pull-down network. Usually, *CL* is the input capacitance of the next node in the dynamic chain, so it is substantially smaller than the input capacitance of the CMOS equivalent. The switching period thus is decreased and becomes similar to the CMOS-design current-sinking capabilities of the pull-down network. This analysis seems somewhat unfair, since it does not take into account the precharge phase. However, it is very often possible to conceal the precharge during other system functions. Figure 2 depicts a comparison of the maximum gate frequency as a function of *V*DD for CMOS, dynamic, and DML chains. First, as expected, the highest frequency is achieved by unfooted dynamic logic. However, dynamic logic is very sensitive to process variations (discussed in Section III-C), which make it unusable for the subthreshold regime. Second, the dynamic DML gates with an average of an order of magnitude have higher-frequency than CMOS. Third, the unfavorable case of consecutive gates of the same type (in this case the chain was composed of interleaved Type A and Type B NAND gates) shows speed degradation of 17%, as compared to the DML chain of consecutive NAND and NOR gates. Fourth, CMOS logic achieves frequency which is lower than the dynamic DML. Fifth, and last, is the static DML, which offers on average 55% of the achievable CMOS frequency. This means that switching from static mode in DML to dynamic mode offers a 14× frequency boost on average, with energy consumption consequences that will be discussed in the following section.

3.2. Energy Dissipation

A simulation of the same chain composed of 20 consecutive NANDNOR demonstrates an energy consumption analysis. We used the test chain to estimate the total energy consumed during one switch.

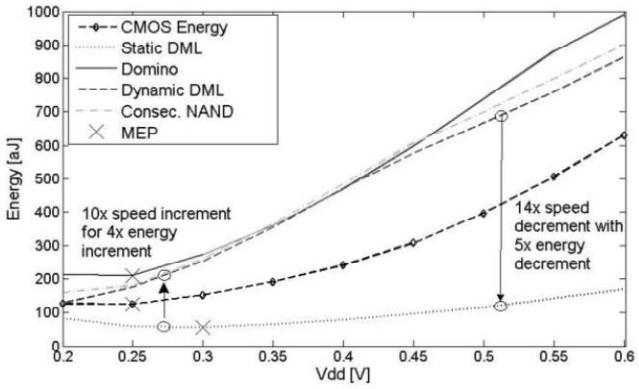


Figure 3. NAND-NOR test chain energy consumption versus VDD for CMOS, Domino, and DML (static and dynamic).

We used only footed dynamic gates, since, as previously noted, an unfooted dynamic gate does not stand process variation. The results of the analysis are shown in Figure 3. *V*DD varies from 0.2 to 0.6 V, and the minimum energy point (MEP) is marked with an "X." The DML static mode demonstrated a lowest energy consumption, on average, 2.2× less than CMOS and 5× less than domino. As can be observed, the MEP for DML gates is located in the subthreshold region. Although it is not always possible, the optimal operation voltage for ultralow power applications is *V*DD*,* MEP at MEP [12]. If *V*DD is higher than *V*DD*,* MEP,

dynamic energy is wasted, and if *V*DD is below *V*DD*,* MEP, leakage energy is wasted, due to the prolonged *T*Cycle [13]. Herein lies an interesting DML feature: the circuit can be tuned to operate at an MEP bound to a certain nominal frequency, but, when required or higher throughput, a higher-frequency can be easily achieved by changing the operation mode to dynamic with an acceptable energy penalty. The opposite is also possible: the circuit can operate at a high-frequency, but at standby the consumed energy can drop down to 20% of the nominal consumption. As expected, domino logic consumes the highest amount of energy, due to the precharging, high leakage, and excessive transistors as keepers.

3.3. Robustness and Sensitivity to Process Variations

The subthreshold regime, while offering low power consumption, suffers from process variation susceptibility and reduction of noise margins. In the following sections, we present two metrics used to quantitatively estimate the robustness of DML logic versus CMOS and domino design. *1) Static Noise Margin (SNM):* The metric to estimate an employed logic gate failure is SNM for logic gates, as introduced by Kwong and Chandrakasan [14]. This metric suggests a simple analysis of the butterfly curve. Logic failure is defined as a butterfly plot SNM analysis with no inscribed square, analogous to a 6T static random-access memory (SRAM) cell displaying negative SNM. In order to test DML we connected a NAND gate to a NOR gate back to back, as it was applied in [15] for an SRAM cell. SNM is defined as the largest inscribed square's side in the smaller lobe of a butterfly plot. We have used this criterion only for the CMOS and the static DML, since dynamic logic and dynamic DML cannot be tested correctly using this analysis. Figure 4 shows the DML and CMOS SNMs at *V*DD = 300 mV. The Monte Carlo analysis for 1 k points, which takes into account both local and global variations, was utilized. The simulated SNM for CMOS is *μ*CMOS = 77 mV, *σ*CMOS = 7.7 mV, and the DML static SNM is *μ*DML = 52 mV and *σ*DML = 11.2 mV. The SNR of the SNM received for CMOS is a little bit higher than the SNR of static DML, which implies higher robustness of CMOS.

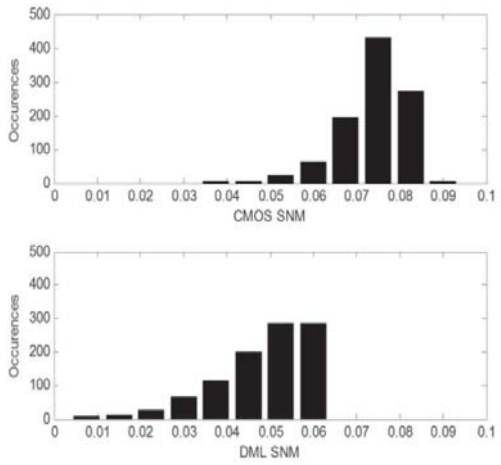


Figure 4. Monte Carlo SNM analysis, VDD = 300 mV. (a) CMOS SNM: *μ*CMOS = 77 m, *σ*CMOS = 7.7 m. (b) DML SNM: *μ*DML = 52 m, *σ*DML = 11.2 m.

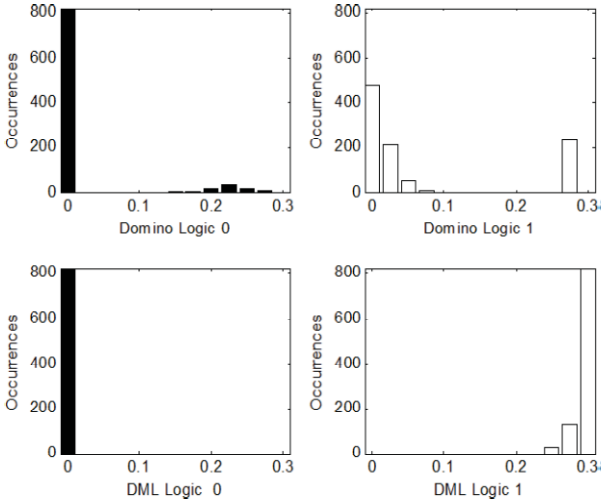


Figure 5. Monte Carlo LL analysis, VDD = 300 mV. (a) Domino LL: *μ*DOMINO−0 = 16.8 m, *σ*DOMINO−0 = 61.3 m. (b) *μ*DOMINO−1 = 89 m, *σ*DOMINO−1 = 118.4 m. DML LL. (c) *μ*DML−0 = 22 m, *σ*DML−0 = 14.2 m. (d) *μ*DML−1 = 299.8 m, *σ*DML−1 = 206 m

However, it can be seen that static DML is still very robust. Moreover, it should be noted that when DML was optimized for improved robustness rather than improved speed, better SNM values were received. In the following section, we will evaluate the dynamic DML versus the domino robustness. *D. Logical Level (LL) Analysis* To evaluate the process variation susceptibility of the dynamic DML and domino, we introduced LL analysis. We used LL analysis

as a framework to evaluate the tested dynamic logic's ability to handle leakage currents. According to the LL analysis, a gate is either precharged to VDD or dis- precharged to 0 V, and after a predefined period, the output voltages of the different gates are compared. Dynamic gates suffer from charge leakage, which becomes more severe in subthreshold due to long static periods. This analysis takes into account all the parasitic leakages and approximates the robustness of the dynamic gate to hold a logical 0 or a logical 1. The test consisted of a single gate in a chain, precharged, and after a period suitable for 10-MHz operation, the voltage was measured at the output of the gate. We tested the DML unfooted gates versus the domino gates with a keeper. We used a keeper since domino gates without a keeper failed to operate. The LL analysis was performed using a 1-k-point Monte Carlo simulation with local and global interdie variations, which simulate a sampling of logic gates across various dies. Figure 5 shows the LL histograms received at VDD = 300 mV. The received results for logical "0" are μDOMINO−0 = 16.8 mV, σDOMINO−0 = 61.3 mV and μDML−0 = 22 mV, and σDML−0 = 14.2 mV. For logical "1": μDOMINO−1 = 89 mV, σDOMINO−1 = 118.4 mV and μDML−1 = 299.8 mV and σDML−1 = 206 μV.

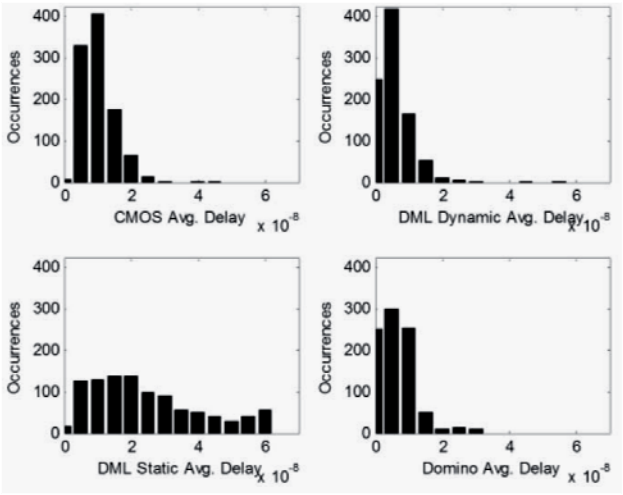


Figure 6. Monte Carlo delay analysis, VDD = 300 mV. (a) DML dynamic mode with footer: μDML_w_footer = 16.22 ns, σDML = 9 ns. (b) omino: Domino = 12.77 ns, σDomino = 13.81 ns. (c) DML static mode: μDML_static = 31 ns, σDML = 17.2 ns. (d) CMOS: μCMOS = 18.8 ns, σCMOS = 8 ns

These results strongly indicate an improved obustness of DML dynamic logic versus standard domino implementation. It can be noted that a fairly large amount of the tested domino gates failed to keep the LL "1," due to the topology which consists of a stack of n-MOS transistors struggling with a feeble p-MOS precharge transistor at some of the simulated dies. We also examined the lowest possible VDD for CMOS, domino, and DML under global and local variations. The results were 285 mV for CMOS, 470 mV for domino, and 300 mV for DML.

3.4. Delay Variation

Obviously, delay variation affects the performance, which thus affects the yield. It is well known that circuits operating in the subthreshold regime exhibit more magnified sensitivity to variations than in the above-threshold. This is due to the exponential dependence of Vth. The common assumption is that Vth is distributed normally, hence, the subthreshold current is log-normally distributed. The delay of a subthreshold logic gate can be modeled as

$$t_d = \frac{K C_g V_{DD}}{I_0 \cdot e^{\frac{(V_{GS}-V_T)}{n\varphi_t}}} \qquad (2)$$

Where *K* is a fitting parameter and *Cg* is the extracted output capacitance. The denominator is the active current, modeled using I0 as a fitting parameter, which takes into account the total current flowing through the n-MOS and p-MOS transistors. Assuming nonvarying output capacitance, we predict that the delay will also be log-normally distributed, since it is linearly related to the on current. Indeed, the 1-*k* Monte Carlo analysis of the average delay yields a log-normal distribution, as depicted in Figure 6. The received results are, from the fastest to the slowest: domino with μDomino = 12.77 ns, DML dynamic mode with μDML_*w*_footer = 16.22 ns, CMOS with μCMOS = 18.8 ns and DML static mode with μDML_static = 31 ns. The domino offers the highest- frequency, but as previously discussed, it suffers greatly from leakage, and consequently exhibits a very low yield. In terms of yield, for example, if the target operation frequency is 10 MHz at 300 mV, Monte Carlo results mean almost 100% yield in the case of the DML, and less than 40% in the domino. Thus, in practice, standard domino logic is unsuitable for the subthreshold regime.

3.5. Test Chip Measurements-Preliminary Proof-of-Concept

In order to provide a preliminary proof-of-concept of the proposed family, we have fabricated two DML test structures as a part of a test chip in a low-power 80-nm TSMC process.

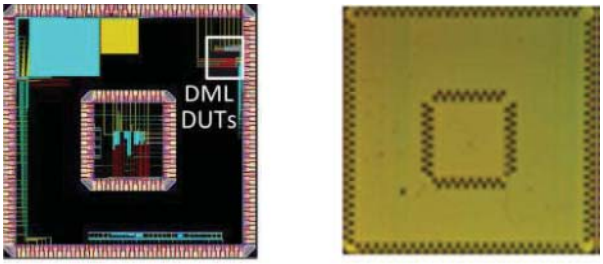
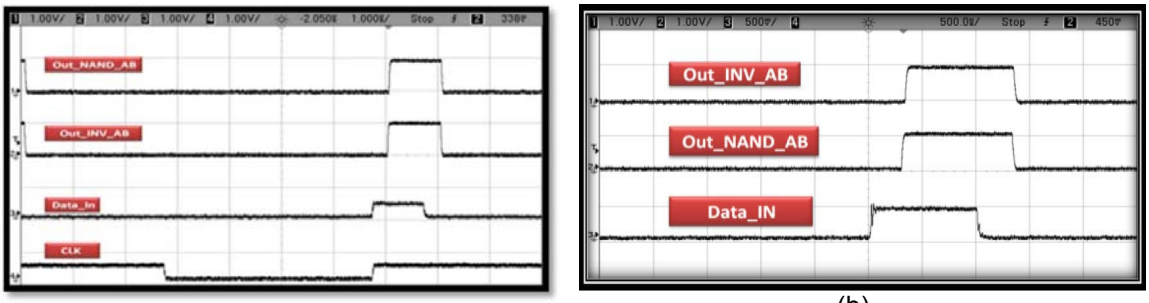


Figure 7. (a) Layout of test chip. (b) Test chip micrograph.



(a) (b)

Figure 8. Measurement results of NAND AB and INV AB and chain at VDD = 400 mV. (a) Dynamic mode. (b) Static mode.

The fabricated DML structures are 100 stage chains with the following architectures: 1) Type A gate followed by a Type B gate, denoted as AB, and 2) Type A gate followed by a CMOS inverter, denoted as AI. Figure 7 shows the layout and die photograph of the test chip, which includes other projects as well. The DML devices under test are marked in Figure 7(a). The chip was covered by metal layers for density reasons. Post-silicon testing was performed with 400 mV– 1.1 V supply voltages at 27 °C. All control signals and biases were generated externally using a Pulse Instruments 4000 Series Test System. Static and dynamic behaviors were measured using the Agilent B1500a semiconductor device analyzer. In Figure 8, we can see positive evidence for the functionality of the DML family. Figure 8(a) shows the waveforms of two different chains: 1) 100 NAND gates connected in AB configuration and 2) 100 DML inverters. The delay we received from both chains is about 20 ns at 400 mV. The static mode

operation, shown in Figure 8(b), was also verified. To activate the static mode, Clk was connected to *V*DD. As expected, both chains behaved as CMOS gates. The measured chain delay was approximately 200 ns, which is about 10× higher than the dynamic operation. Comparison between simulation and measurement results, which is not presented in this brief due to length limitations, showed coherence between simulated and measured results with an average and maximum differences of 13% and 25%, respectively.

4. Conclusion

In this brief, we presented a novel family, DML, which was shown for subthreshold operation. We showed that the DML dynamic mode presented an average 10× speed improvement as compared to CMOS, and improved robustness as compared to a standard dynamic logic.

The DML static mode demonstrated the lowest energy dissipation: 2.2× less than CMOS on average, and 5× less than the domino. We presented a basic proof-of-concept of the proposed DML logic by measurements of an 80-nm test chip. Future work will include the optimization of the DML gates for operation with standard supply voltages, development of a standard library and designing of a benchmark design using a standard ASIC flow.

Acknowledgment

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